L17 ANSWER 15 OF 48 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 2004:352782 CAPLUS
DOCUMENT NUMBER: 140:367027
TITLE: **Epitaxial** CoSi2 on MOS devices
INVENTOR(S): Lim, Chong Wee; Shin, Chan Soo; Petrov, Ivan Georgiev; Greene, Joseph E.
PATENT ASSIGNEE(S): The Board of Trustees of the University of Illinois, USA
SOURCE: U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2004079279	A1	20040429	US 2002-280668	20021025
US 6846359	B2	20050125		
PRIORITY APPLN. INFO.:			US 2002-280668	20021025

AB An SixNy or SiOxNy liner is formed on a MOS device. Co is then deposited and reacts to form an **epitaxial** CoSi2 layer underneath the liner. The CoSi2 layer may be formed through a solid phase **epitaxy** or reactive deposition **epitaxy** salicide process. In addition to high quality **epitaxial** CoSi2 layers, the liner formed during the invention can protect device portions during etching processes used to form device contacts. The liner can act as an etch stop layer to prevent excessive removal of the shallow **trench** isolation, and protect against excessive loss of the CoSi2 layer.

IT **682344-31-6P**, Silicon nitride oxide (SiN0.01-1.33O)
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); PROC (Process); USES (Uses)
(**epitaxial** cobalt silicide formation on MOS devices)
RN 682344-31-6 CAPLUS
CN Silicon nitride oxide (SiN0.01-1.33O) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	0.01 - 1.33	17778-88-0
O	1	17778-80-2
Si	1	7440-21-3

REFERENCE COUNT: 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 16 OF 48 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 2004:328381 CAPLUS
DOCUMENT NUMBER: 141:43408
TITLE: Novel interface structures between ultrathin oxynitride and Si(001) studied by X-ray diffraction
AUTHOR(S): Takahashi, Isao; Kada, Tositeru; Inoue, Kouji; Kitahara, Amane; Shimazu, Hiromitsu; Tanaka, Norihisa; Terauchi, Hikaru; Doi, Syuichi; Nomura, Kenji; Awaji, Naoki; Komiya, Satoshi
CORPORATE SOURCE: Advanced Research Center of Science, Faculty of Science and Technology, Kwansei Gakuin University (ARCS-KGU), Sanda, 669-1337, Japan
SOURCE: Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (2003), 42(12), 7493-7496
CODEN: JAPNDE
PUBLISHER: Japan Society of Applied Physics
DOCUMENT TYPE: Journal
LANGUAGE: English

AB For ultrathin oxynitride layers 2.4 nm thick, x-ray crystal truncation rod (CTR) scattering is conducted to study the interface structures between oxynitride and Si(001). (004) And (202)CTRs showed that the [amorphous oxide]/Si(001) interface is hardly varied by NO-nitrided oxynitridation. However, (111)CTR indicated that **epitaxial** oxide crystallites in the matrix of amorphous oxide layer are significantly affected by N: probably N atoms at the interface are captured by these crystallites after their migration on the interface. As interstitial atoms, the adsorbed N makes the crystallites amorphous. Such an annihilation of the crystallites should be responsible for the high performance of oxynitride as **gate** oxides. Further oxynitridation where the N concentration reaches 4 atomic% showed a distinct variation in (111)CTR, indicating the creation of a novel structural order at the interface. Such a structural order probably is **nucleated** by the excessively concentrated N. A close relation between the novel structural order and degradation of the over-oxynitrided layers is strongly suggested.

REFERENCE COUNT: 23 THERE ARE 23 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 33 OF 48 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 2001:422530 CAPLUS
DOCUMENT NUMBER: 135:188305
TITLE: Nitrided thermal SiO2 for use as top and bottom **gate** insulators in self-aligned double **gate** silicon-on-insulator metal-oxide-semiconductor field effect transistor mosfet
AUTHOR(S): Ahmed, Shibly S.; Denton, John P.; Neudeck, Gerold W.
CORPORATE SOURCE: School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, 47907, USA
SOURCE: Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (2001), 19(3), 800-806
CODEN: JVTBD9; ISSN: 0734-211X
PUBLISHER: American Institute of Physics
DOCUMENT TYPE: Journal
LANGUAGE: English
AB Nitrided thermal oxide was used to reduce the degradation of top and bottom **gate** insulators of self-aligned double **gate** metal-oxide-semiconductor field effect transistors that use a form of selective **epitaxial** growth of silicon (SEG) called tunnel **epitaxy**. SOI. The degradation of thermal oxide was due to the exposure of **gate** insulator to the epi-growth ambient gases during the **epitaxial** growth. Both thermal oxide and thermally nitrided oxide samples were exposed to the epi-reactor gases and then the elec. characteristics were measured. Nitrided oxide showed significantly higher breakdown field, lower leakage current, and lower interface states than the thermal oxide after exposure to the selective epi-growth environment. For a 30 min stress in epi-reactor ambient, thermal oxide showed average breakdown fields of less than 1 MV/cm due to the formation of pinholes, while nitrided oxide samples showed average breakdown fields of 15.6 MV/cm for same stress condition. Interface state d. (Dit) of nitrided oxide improved after exposure to **epitaxial** growth ambient. The average Dit reduced from .apprx.3.5+1010/cm2 eV to .apprx.1.5+1010/cm2 eV for a 30 min SEG/**epitaxial** lateral overgrowth stress for nitrided oxides.
REFERENCE COUNT: 35 THERE ARE 35 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 37 OF 48 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 2000:639155 CAPLUS
DOCUMENT NUMBER: 133:216540
TITLE: Method of forming transistor having an improved sidewall **gate** structure
INVENTOR(S): Chatterjee, Amitava; Lee, Wei William; Hames, Greg A.; He, Quzhi; Ali, Iqbal; Hanratty, Maureen A.
PATENT ASSIGNEE(S): Texas Instruments Incorporated, USA
SOURCE: U.S., 8 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.		DATE
US 6117741	A	20000912	US 1999-226237		19990105
US 6307230	B1	20011023	US 1999-416380		19991012
PRIORITY APPLN. INFO.:			US 1998-70982P	P	19980109
			US 1999-226237	A3	19990105

AB A transistor having an improved sidewall **gate** structure and method of fabrication is provided. The improved sidewall **gate** structure may include a semiconductor substrate having a **channel** region. A **gate** insulation may be formed adjacent to the **channel** region of the semiconductor substrate. A **gate** may be formed adjacent to the **gate** insulation. A sidewall insulation body may be formed adjacent to a portion of the **gate**. The sidewall insulation body is composed of a **silicon oxynitride** material. An **epitaxial** layer may be formed adjacent to a portion of the sidewall insulation body and adjacent to the semiconductor substrate substantially outward of the **channel** region. A buffer layer may be formed adjacent to a portion of the sidewall insulation body and adjacent to the **epitaxial** layer.
REFERENCE COUNT: 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 42 OF 48 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1997:590952 CAPLUS
DOCUMENT NUMBER: 127:184279
TITLE: Production of semiconductor integrated circuits
INVENTOR(S): Wada, Shigemi
PATENT ASSIGNEE(S): NEC Corp., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09186174	A2	19970715	JP 1995-341726	19951227
JP 2914429	B2	19990628		

PRIORITY APPLN. INFO.: JP 1995-341726 19951227

AB The title process involves forming an insulator film on a 1st conductivity-type semiconductor substrate, opening a 1st. contact hole, selectively **epitaxying** a 2nd conductivity-type semiconductor crystal film in the hole over the insulator as its mask to give a **gate** electrode in a junction-type 1st field-effect transistors, opening a 2nd contact hole to the insulator film, and depositing a metal in the contact hole to give a **gate** electrode for a Schottky-barrier 2nd field-effect transistor. The 1st and 2nd **gate** electrodes give the 1st and 2nd transistors as driving and load transistors for the semiconductor integrated circuits.

IT **132614-63-2P**, Silicon nitride oxide (SiNO)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); PROC (Process); USES (Uses)
(production of semiconductor integrated circuits)
RN 132614-63-2 CAPLUS
CN Silicon nitride oxide (Si(N,O)) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	0 - 1	17778-88-0
O	0 - 1	17778-80-2
Si	1	7440-21-3

L17 ANSWER 43 OF 48 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1997:184469 CAPLUS
DOCUMENT NUMBER: 126:179890
TITLE: Semiconductor integrated circuit devices and manufacture thereof
INVENTOR(S): Toida, Takashi; Aihara, Katsuyoshi
PATENT ASSIGNEE(S): Citizen Watch Co Ltd, Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 19 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09008309	A2	19970110	JP 1995-147953	19950615
PRIORITY APPLN. INFO.:			JP 1995-147953	19950615

AB The title process comprises sequential formation of an insulating and a Si oxynitride film on a Si substrate, formation of a polycryst. Si lower **gate** electrode and a lower **gate** insulating film thereon, removal of the Si oxynitride and the insulating film on a **seed** region and cleaning of exposed substrate surface, deposition of an amorphous Si film on the entire surface, formation of an active layer by **epitaxy** therefrom in N2 atmospheric, division of the active layer into islands, sequential formation of an upper **gate** insulating film, an upper **gate** electrode, and the source-**drain** region for preparation of a double-**gate** field-effect thin-film transistor. The active region has a stable interface with the Si oxynitride film, and solid phase growth distance of the Si film can be extended and voltage resistance of the **gate** insulating film is raised.

L17 ANSWER 44 OF 48 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1996:260992 CAPLUS
DOCUMENT NUMBER: 124:357312
TITLE: TEM observation of defects induced by nitrogen annealing on a Si(100) surface
AUTHOR(S): Sadamitsu, S.; Yamamoto, T.; Sumita, S.; Shigematsu, T.
CORPORATE SOURCE: Silicon Technol. R D Cent., Sumitomo Sitix Corp., Saga, 849-05, Japan
SOURCE: Electron Microscopy 1994, Proceedings of the International Congress on Electron Microscopy, 13th, Paris, July 17-22, 1994 (1994), Volume 2A, 109-10. Editor(s): Jouffrey, Bernard; Colliex, C. Editions de Physique: Les Ulis, Fr.
CODEN: 62SHAV
DOCUMENT TYPE: Conference
LANGUAGE: English

AB The behavior of surface defects induced by high temperature annealing in N2 was investigated by TEM. The formation of amorphous SiNxOy ppts. near the surface of Si(100) wafers during high temperature heat treatment in N2 was observed using TEM. The degradation of the **gate** oxide integrity yield after such heat treatments is believed to be caused by the formation of these defects near the Si(100) surface. These defects were also show to act as **nucleation** sites for oxidation stacking faults during subsequent thermal oxidation

IT **132614-63-2**, Silicon nitride oxide (Si(N,O))
RL: FMU (Formation, unclassified); MOA (Modifier or additive use); FORM (Formation, nonpreparative); USES (Uses)
(precipitation of **silicon oxynitride** near silicon (100) surface during annealing in relation to **gate** oxide integrity)

RN 132614-63-2 CAPLUS
CN Silicon nitride oxide (Si(N,O)) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	0 - 1	17778-88-0
O	0 - 1	17778-80-2
Si	1	7440-21-3

L17 ANSWER 46 OF 48 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1995:967711 CAPLUS
DOCUMENT NUMBER: 124:73923
TITLE: Manufacture of field-effect transistor (FET) on compound semiconductor substrate
INVENTOR(S): Kuroda, Atsushi; Ooshika, Katsushi
PATENT ASSIGNEE(S): Hitachi Ltd, Japan; Hitachi Vlsi Eng
SOURCE: Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 07249638	A2	19950926	JP 1994-37396	19940308
PRIORITY APPLN. INFO.:			JP 1994-37396	19940308

AB The FET is manufactured by forming a **gate** electrode on a substrate, CVD of a 1st insulating film (oxynitride: n = 1.60±0.05) on the substrate, ion implantation into the substrate using the 1st oxynitride film as a protective film, forming sidewall spacers of the **gate** electrode with a 2nd insulating film (oxynitride: n = 1.60±0.05), annealing the substrate to diffuse the impurities, and selective **epitaxial** growth of a semiconductor layer containing high-concentration impurities in the diffusion regions to form source/**drain**. The process is applicable to manufacture of a HIGFET (heterostructure insulated **gate** FET). The FET has stable Schottky property.

L17 ANSWER 41 OF 48 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 1999:316450 CAPLUS
DOCUMENT NUMBER: 130:319540
TITLE: Fabrication of a stacked Si **gate** p-MOSFET having an elevated and extended source-**drain** junction
INVENTOR(S): Wu, Shye-lin
PATENT ASSIGNEE(S): Texas Instruments--Acer Incorporated, Taiwan
SOURCE: U.S., 8 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5902125	A	19990511	US 1997-999268	19971229
PRIORITY APPLN. INFO.:			US 1997-999268	19971229

AB The invention relates to a process for making a stacked Si **gate** p-MOSFET having an elevated and extended source-**drain** junction. A stacked-amorphous-silicon (SAS) layer is then formed on the **gate** oxide. An anti-reflective coating (ARC) layer is formed on the SAS layer. Next, a **gate** structure is patterned by etching. A **silicon oxynitride** layer is formed on the substrate, and covered the **gate** structure. A BSG sidewall spacers are formed on the side walls of the **gate** structure. A selective **epitaxial** silicon is grown on the substrate by using ultra high vacuum chemical vapor deposition. Then, an ARC layer is removed to expose the top of the SAS layer. Then, a blanket ion implantation is carried out to implant p type dopant into the SAS layer, the **epitaxial** silicon and silicon substrate. A SALICIDE layer, a polycide layer are resp. formed on the SAS layer and the **epitaxial** silicon. Further, the extended source and **drain** are formed in the step. A thick oxide layer is formed over the substrate and **gate** structure for isolation. Then, contact holes are generated in the oxide layer. Next, a metalization is carried out to form elec. connecting structure over the contact holes.

REFERENCE COUNT: 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

$Si_xO_yN_z$ on gate structure + beneath
Spacer - not used for SEG.

L21 ANSWER 3 OF 4 CAPLUS COPYRIGHT 2005 ACS on STN
ACCESSION NUMBER: 2003:42723 CAPLUS
DOCUMENT NUMBER: 138:82007
TITLE: Process for selective epitaxial growth and bipolar transistor made by using such process
INVENTOR(S): Chevalier, Pascal Guy Yves; De Pestel, Freddy Marcel Yvan; Ackaert, Jan; Vastmans, Johan
PATENT ASSIGNEE(S): Alcatel, Fr.
SOURCE: U.S. Pat. Appl. Publ., 7 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2003011001	A1	20030116	US 2002-194053	20020715
EP 1280189	A1	20030129	EP 2001-401908	20010716
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR				
TW 574729	B	20040201	TW 2002-91114767	20020703
JP 2003045886	A2	20030214	JP 2002-200794	20020710
PRIORITY APPLN. INFO.:			EP 2001-401908 A	20010716

AB The invention relates to a process for the selective epitaxial growth of a Si-containing layer (e.g., Si or SiGe) on a substrate, characterized in that the substrate is provided with a layer of **silicon oxynitride** with an atomic concentration of oxygen between 30 and 45% and an atomic concentration of nitrogen between 19 and 35% before the selective epitaxial growth of the Si-containing layer.

teaches using $Si_xO_yN_z$ to mask a SEG, not seed.